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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent No. 6,934,349	)	Serial No. 09/955,131
	)	
Inventor(s): Tomoaki YABE	)	Filed: September 19, 2001
	)	
Issue Date: August 23, 2005	)	Attorney Docket No. 0002372.00031

For: PHASE DETECTOR AND PHASE LOCKED LOOP CIRCUIT

REQUEST FOR CERTIFICATE OF CORRECTION

U.S. Patent and Trademark Office
Customer Service Window
Randolph Building, Mail Stop: Certificate of Correction Branch
401 Dulany Street
Alexandria, VA 22314

Sir:

Pursuant to 35 U.S.C. § 254 and 37 C.F.R. § 1.322, this is a request for the issuance of a Certificate of Correction in the above-identified patent. Two (2) copies of PTO Form 1050 are appended. The complete Certificate of Correction involves one page.

The mistakes identified in the appended Form occurred through no fault of the Applicant, as clearly disclosed by the records of the application, which matured into this patent. Enclosed for your convenience are the relevant portions of the Examiner's Amendment enclosed with the Notice of Allowance dated April 22, 2005 and the Amendment filed February 22, 2005.

Issuance of the Certificate of Correction containing the corrections is respectfully requested. Applicants believe these errors were caused by the Office's copying of the claims with clerical errors. Therefore, we believe no fee to be associated with this request. Nonetheless, should the Patent and Trademark Office determine these errors to be Applicants such that a fee is required, please charge our Deposit Account No. 19-0733.

Respectfully submitted,

BANNER & WITCOFF, LTD.

Dated: March 6, 2006

By: _____
Gary D. Fedorochko
Registration No. 35,509

1001 G Street, N.W. (11th Fl.)
Washington, D.C. 20001
(202) 824-3000

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.: 6,934,349

DATED: August 23, 2005

INVENTOR(S): Tomoaki YABE

It is certified that errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In Column 6, Claim 1, Line 12:
Please replace "the se state" with --the set state--

In Column 6, Claim 1, Line 16:
Please replace "logic ad said" with --logic and said--

In Column 6, Claim 2, Line 26:
Please replace "configured t bring" with --configured to bring--

In Column 7, Claim 9, Line 49:
Please replace "logic ad said" with --logic and said--

In Column 7, Claim 10, Line 59:
Please replace "configured t bring" with --configured to bring--

Mailing Address of Sender:

Banner & Witcoff, Ltd.
11th Floor
1001 G Street, N.W.
Washington, DC 20001-4597

FORM PTO 1050 (Rev.2-93)

U.S. PAT. NO 6,934,349

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NOTICE OF ALLOWANCE AND FEE(S) DUE

22907 7590 04/22/2005

BANNER & WITCOFF
1001 G STREET N W
SUITE 1100
WASHINGTON, DC 20001

EXAMINER
JOSEPH, JAISON

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 04/22/2005

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/955,191	09/19/2001	Tomoaki Yabe	02372.00031	8398

TITLE OF INVENTION: PHASE DETECTOR AND PHASE LOCKED LOOP CIRCUIT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$1700	07/22/2005

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should be completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

Notice of Allowability	Application No.	Applicant(s)	
	09/955,131	YABE, TOMOAKI	
	Examiner	Art Unit	
	Jaison Joseph	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed on February 28, 2005*.

2. ☒ The allowed claim(s) is/are *4 -11 and 15 - 20, renumbered 1 - 8 and 9 - 14, respectively*.

3. ☒ The drawings filed on *19 September 2001* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Gary D. Fedoeochko on 04/08/2005.

The application has been amended as follows:

Claim 4 rewrite as: A phase detector configured to output an up signal when a first clock signal is ahead of a second clock signal in phase, and outputting a down signal when said first clock signal is behind said second clock signal in phase, said phase detector comprising: first, second, and third flip-flops; a flip-flop (F/F) control circuit which brings said first flip-flop to a reset state when at least one of said first and second clock signals has a first logic, brings said first flip-flop to a set state when both said second and third flip-flops are in the set state, brings said second flip-flop to the set state when said first clock signal has a second logic and said first flip-flop is in the reset state, brings said second flip-flop to the reset state when both said second and third flip-flop are in set state, brings said third flip-flop to the set state when said second clock signal has a second logic ad said first flip-flop is in reset state, and brings said third flip-flop to the reset state when both said second and third flip-flops are in the set state; and an up-down signal output circuit configured to output said up signal and down signal based on the outputs of said second and third flip-flops.

Claim 5 rewrite as: The phase detector according to claim 4 wherein said flip-flop (F/F) control circuit comprises: a first logic circuit configured to reset said first flip-flop when at least one of said first and second clock signals has said first logic; a second logic circuit configured to bring said second flip-flop to the set state when said flip-flop is in the reset state and said first clock signal had said second logic; a third logic circuit configured to bring said third flip-flop to the set state when said first flip-flop is in the reset state and said second clock signal has said second logic; a fourth logic circuit configured to bring said second and third flip-flop to the reset state when said second and third flip-flops are in the set state; a fifth logic circuit configured to output an up signal when said second flip-flop is in the set state and third flip-flop is in the reset state; and a sixth logic circuit configured to output said down signal when said third flip-flop is in the set state and said second flip-flop is in the reset state.

Claim 15 rewrite as: A phase locked loop circuit comprising: a charge pump configured to output a voltage signal in accordance with an up signal and a down signal; a loop filter configured to remove a high frequency component included in the an output of said charge pump; a voltage control oscillation circuit configured to output a signal of a frequency in accordance with output voltage of said loop filter; a clock buffer configured to output a clock signal in accordance with an output of said voltage control oscillation circuit; and a phase detector configured to output the up signal when a first clock signal is ahead of a second clock signal in phase, and outputting a down signal when said first clock signal is behind said second clock signal in phase, wherein said phase detector comprises: first, second, and third flip-flops; a flip-flop (F/F) control

circuit which brings said first flip-flop to a reset state when at least one of said first and second clock signals has a first logic, brings said first flip-flop to a set state when both said second and third flip-flops are in the set state, brings said second flip-flop to the set state when said first clock signal has a second logic and said first flip-flop is in the reset state, brings said second flip-flop to the reset state when both said second and third flip-flop are in set state, brings said third flip-flop to the set state when said second clock signal has a second logic ad said first flip-flop is in reset state, and brings said third flip-flop to the reset state when both said second and third flip-flops are in the set state; and an up-down signal output circuit configured to output said up signal and down signal based on the outputs of said second and third flip-flops.

Claim 16 rewrite as: The phase locked loop circuit according to claim 4 wherein said flip-flop (F/F) control circuit comprises: a first logic circuit configured to reset said first flip-flop when at least one of said first and second clock signals has said first logic; a second logic circuit configured t bring said second flip-flop to the set state when said flip-flop is in the reset state and said first clock signal had said second logic; a third logic circuit configured to bring said third flip-flop to the set state when said first flip-flop is in the reset state and said second clock signal has said second logic; a fourth logic circuit configured to bring said second and third flip-flop to the reset state when said second and third flip-flops are in the set state; a fifth logic circuit configured to output an up signal when said second flip-flop is in the set state and third flip-flop is in the reset state; and a sixth logic circuit configured to output said down signal when said third flip-flop is in the set state and said second flip-flop is in the reset state.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:		Atty. Docket No.:	002372.00031
Tomoaki YABE			
Serial No.:	09/955,131	Group Art Unit:	2634
Filed:	September 19, 2001	Examiner:	Joseph, J.
For:	PHASE DETECTOR AND PHASE LOCKED LOOP CIRCUIT	Confirmation No.:	8398

AMENDMENT

U.S. Patent and Trademark Office
Customer Service Window, Mail Stop Amendment
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Sir:

In response to the Office Action mailed November 30, 2004, please amend the instant application as follows:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are reflected in the Listing of Claims, which begins on page 4 of this paper.

Remarks/Arguments begin on page 10 of this paper.

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-3 (canceled)

Claim 4 (currently amended): ~~The phase detector according to claim 3~~ A phase detector configured to output an up signal when a first clock signal is ahead of a second clock signal in phase, and outputting a down signal when said first clock signal is behind said second clock signal in phase, said phase detector comprising:

first, second and third flip-flops;

~~wherein said~~ an F/F control circuit which brings said first flip-flop to ~~the~~ a reset state when at least one of said first and second clock signals has a first logic, brings said first flip-flop to ~~the~~ a set state when both said second and third flip-flops are in the set state, brings said second flip-flop to the set state when said first clock signal has a second logic and said first flip-flop is in the reset state, brings said second flip-flop to the reset state when both said second and third flip-flops are in the set state, brings said third flip-flop to the set state when said second clock signal has the second logic and said first flip-flop is in the reset state, and brings said third flip-flop to the reset state when both said second and third flip-flops are in the set state; and

an up/down signal output circuit configured to output said up signal and the down signal based on the outputs of said second and third flip-flops.

Claim 5 (original): The phase detector according to claim 4 wherein said F/F control circuit comprises:

a first logic circuit configured to reset said first flip-flop when at least one of said first and second clock signals has said first logic;

a second logic circuit configured to bring said second flip-flop to the set state when said first flip-flop is in the reset state and said first clock signal has said second logic;

a third logic circuit configured to bring said third flip-flop to the set state when said first flip-flop is in the reset state and said second clock signal has said second logic;

a fourth logic circuit configured to bring said second and third flip-flops to the reset state when both said second and third flip-flops are in the set state;

a fifth logic circuit configured to output said up signal when said second flip-flop is in the set state and said third flip-flop is in the reset state; and

a sixth logic circuit configured to output said down signal when said third flip-flop is in the set state and said second flip-flop is in the reset state.

Claim 6 (original): The phase detector according to claim 5 wherein said first flip-flop is brought to the reset state when an output of said first logic circuit has the first logic, and brought to the set state when the output of said fourth logic circuit has said first logic;

said second flip-flop is brought to the set state when the output of said second logic circuit has said first logic, and brought to the reset state when the output of said fourth logic circuit has said first logic, and

said third flip-flop is brought to the set state when the output of said third logic circuit has said first logic, and brought to the reset state when the output of said fourth logic circuit has said first logic.

Claim 7 (original): The phase detector according to claim 6 wherein each of said first, second and third flip-flops comprises a set input terminal, a reset input terminal, and first and second NAND gates,

said first NAND gate performs a NAND operation between the set input terminal and an output terminal of said second NAND gate,

said second NAND gate performs the NAND operation between the reset input terminal and the output terminal of said first NAND gate, and

the output of said first NAND gate forms respective outputs of said corresponding first, second and third flip-flops.

Claim 8 (original): The phase detector according to claim 6 wherein said first logic is a high level, and said second logic is a low level.

Claim 9 (original): The phase detector according to claim 5 wherein said first flip-flop is brought to the reset state when an output of said first logic circuit has said second logic, and brought to the set state when the output of said fourth logic circuit has said second logic;

said second flip-flop is brought to the set state when the output of said second logic circuit has said second logic, and brought to the reset state when the output of said fourth logic circuit has said second logic, and

said third flip-flop is brought to the set state when the output of said third logic circuit has said second logic, and brought to the reset state when the output of said fourth logic circuit has said second logic.

Claim 10 (original): The phase detector according to claim 9 wherein each of said first, second and third flip-flops comprises a set input terminal, a reset input terminal, first and second NOR gates, and an inverter,

said first NOR gate performs a NOR operation between the set input terminal and an output terminal of said second NOR gate,

said second NOR gate performs the NOR operation between the reset input terminal and the output terminal of said first NOR gate,

said inverter reverses an output of said first NOR gate, and

the output of said inverter forms respective outputs of said corresponding first, second and third flip-flops.

Claim 11 (original): The phase detector according to claim 9 wherein said first logic is a high level, and said second logic is a low level.

Claims 12-14 (canceled)

Claim 15 (currently amended): ~~The phase locked loop circuit according to claim 12 wherein~~ A phase locked loop circuit comprising:

a charge pump configured to output a voltage signal in accordance with an up signal and a down signal;

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a loop filter configured to remove a high frequency component included in an output of said charge pump;

a voltage control oscillation circuit configured to output a signal of a frequency in accordance with an output voltage of said loop filter;

a clock buffer configured to output a clock signal in accordance with an output of said voltage control oscillation circuit; and

a phase detector configured to output the up signal when a fist clock signal is ahead of a second clock signal in phase, and outputting a down signal when said first clock signal is behind said second clock signal in phase,

wherein said phase detector comprises:

first, second and third flip-flops;

~~said~~ an F/F control circuit which brings said first flip-flop to a reset state when at least one of said first and second clock signals has a first logic, brings said first flip-flop to a set state when both said second and third flip-flops are in the set state, brings said second flip-flop to the set state when said first clock signal has a second logic and said first flip-flop is in the reset state, brings said second flip-flop to the reset state when both said second and third flip-flops are in the set state, brings said third flip-flop to the set state when said second clock signal has the second logic and said first flip-flop is in the reset state, and brings said third flip-flop to the reset state when both said second and third flip-flops are in the set state; and

an up/down signal output circuit configured to output the up signal and the down signal based on the outputs of said second and third flip-flops.

Claim 16 (original): The phase locked loop circuit according to claim 15 wherein said F/F control circuit comprises:

a first logic circuit configured to reset said first flip-flop when at least one of said first and second clock signals has said first logic;

a second logic circuit configured to bring said second flip-flop to the set state when said first flip-flop is in the reset state and said first clock signal has said second logic;